In the Claims

Please cancel Claims 1-6 and 9-16 without prejudice. Applicant reserves the right to pursue the subject matter of Claims 1-6 and 9-16 in continuation applications.

1-6. (Canceled).

7. (Currently Amended) In an integrated circuit formed on a p-type substrate, an output driver circuit coupled between an internal circuit on the integrated circuit and an input/output pad on the integrated circuit comprising:

a first transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

a second transistor including:

an n-well disposed in said p-type substrate, a portion of said n-well more lightly doped than the remainder of said n-well;

a P+ drain region disposed in said lightly-doped region of said n-well, a periphery of said P+ drain region extending beyond an outer boundary of said lightly-doped region of said n-well, said periphery surrounded by a lightly-doped P region;

a pair of P+ source regions spaced apart from opposite edges of said P+ drain region at a distance sufficient to form first and second channels, each of said P+ source regions surrounded by a lightly doped P region and electrically coupled together;

a first gate region disposed above and insulated from said first channel; and

a second gate region disposed above and insulated from said second channels and electrically coupled to said first gate;

wherein said drain of said first transistor and said drain of said second transistor are coupled to said input output pad, said source regions of said first transistor are coupled to ground, said source regions of said second transistor are coupled to a supply potential, and said gate regions of said first transistor and said second transistor are coupled to an output of said internal circuit.

8. (Original) The output driver circuit of claim 7 wherein:

in said first transistor said periphery of said N+ drain region extends laterally into said p-well beyond said outer boundary of said substrate-doped portion of said p-well a distance about equal to that of said first and second channels of said first transistor; and

in said second transistor said periphery of said P+ drain region extends laterally into said p-well beyond said outer boundary of said lightly-doped region of said n-well a distance about equal to that of said first and second channels of said second transistor.

9-21. (Canceled).